A 6 WATT 6 GHz GaAsFET POWER MODULE WITH GaAs MATCHING CIRCUITS

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SUMMARY

A GaAs matched FET (M-FET) technology has been developed which incorporates separate GaAs matching chips and GaAsFETs within a small hermetic package. By using two separately matched 6 mm FET chips in the design, we have achieved 6.3 watts of output power with 9 dB associated gain at 6 GHz.

INTRODUCTION

The M-FET (Matched Field Effect Transistor) (Fig. 1) is a new approach to an integrated amplifying module. It uses one or more GaAsFET chips for its active elements and has matching and bias circuits fabricated on GaAs. The M-FET combines the attractive features of both monolithic integration and conventional external matching circuits.

- Since all the circuits are on GaAs, full or partial monolithic integration could be employed at a later date to optimize price and performance.
- The circuits are separate from the active device. Thus, circuit changes are quickly and easily made and the time required to modify the module is less than would be required for a monolithic design.
- The separation of circuits and active devices, along with tuning adjustability of the circuits, facilitates adaptability of the module to variations in active device parameters. This is particularly important for a high power module. In general monolithic circuits have had performance difficulties in high power applications.
- The use of GaAs as the substrate material allows considerable flexibility in substrate thickness and, thus, in the selection of the characteristic impedance for matching elements. This leads to simple circuit configurations.
- A further advantage of using GaAs substrates is that full GaAs technology capabilities [1] such as via holes and MIM capacitors can be used in the circuits.

The M-FET module is contained in a hermetic package which may be inserted into a standard 50 ohm transmission line system without external matching and biasing circuitry.

CIRCUIT CONSTRUCTION

For the 6 GHz M-FET the 1 dB bandwidth objective was set at 500 MHz. The GaAsFETs which are being used have input and output impedances which allow the intended bandwidth to be achieved with circuits having a single resonance, sometimes called single-tuned circuits. This means that the Q of the transistor is sufficiently low that a matching circuit consisting of a single inductor and a single capacitor at both input and output ports will transform the impedance of the transistor over the desired bandwidth for operation in a 50 ohm system. Since it is difficult to obtain a pure capacitor or a pure inductor at 6 GHz, these lumped elements have been replaced in the practical designs with the most nearly equivalent distributed elements.

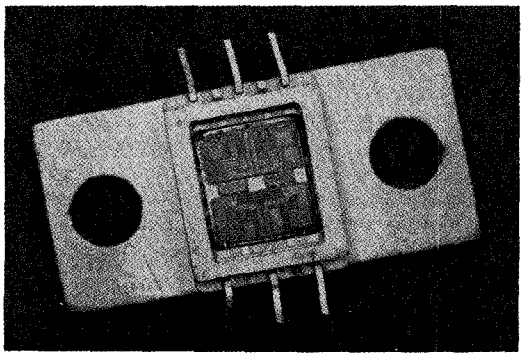

Fig. 1 Matched Field Effect Transistor

In the present circuit design the input circuit consists of a transmission line transformer followed by an open- circuited stub. Gate bias is brought in through a quarter-wave transformer. The output circuit is similar to the input circuit, but instead of the open-circuited stub, a short-circuited stub is used to provide the desired RF properties and facilitate the introduction of drain bias.

The matching circuits, 2.5 mm x 5.0 mm chips, are constructed on 100 micron thick GaAs substrates (Fig. 2). This thickness was selected to obtain low loss while retaining the ability to construct

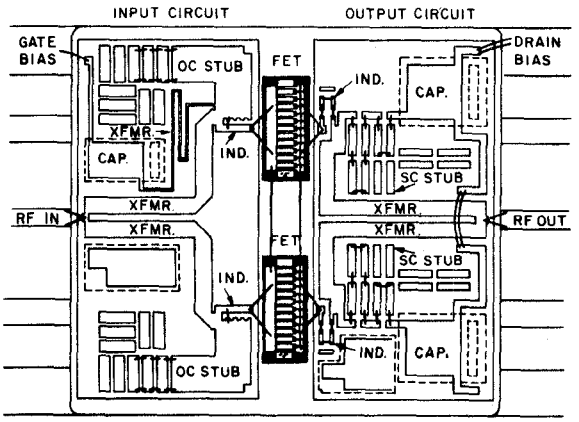

Fig. 2 6 GHz M-FET Circuit Layout

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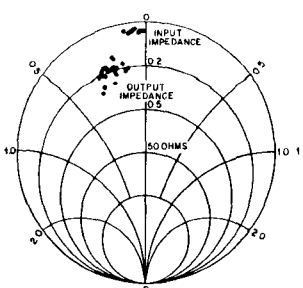
reasonable width, low impedance lines which are necessary for matching the low impedance active devices to 50 ohms. In the present design the widest line has a characteristic impedance of about 15 ohms and the circuit loss is about 1 dB, divided equally between the input and output circuits.

For the 6 GHz M-FET the tuning elements are all of the distributed type and overlay type capacitors are used for RF bypass in the bias circuits. The circuits consist of two layers of metal, each 2 microns thick, separated by a 0.5 micron thick layer of silicon nitride, all on the GaAs substrate. The lower layer of metal, which forms the grounded plate of the bypass capacitors, is connected through the substrate to ground with plated via connections [2]. The upper layer of metal contains all the critical circuit features, the line transformers and stubs used for the RF matching.

CIRCUIT ADJUSTABILITY

Means of making adjustments to the circuits have been incorporated into the design. These adjustments, made by discretionary bonding of trim pads, are used to accommodate the manufacturing tolerances of the GaAsFETs and also to allow fine adjustment of such parameters as linearity and efficiency.

For the first step in designing adjustability into the circuits several transistors similar to those which were to be used in the module were measured to determine the range of their input and output large signal impedances (Fig. 3a). Then, the extremes of the reactive and real parts of those measured impedances were enclosed in an impedance window (Fig. 3b) formed by the range of the impedances of the appropriate adjustable circuit elements. Extra room was left in the window to accommodate adjustment of those other parameters mentioned above.



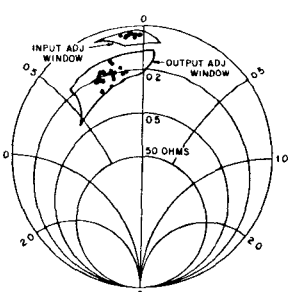


Fig. 3a GaAs FET Impedances Fig. 3b Circuit Impedance Windows

CELL COMBINING IN LARGE POWER M-FETs

The best operation of large power M-FETs was achieved by separating the active device into chips of not more than six or eight millimeters of GaAsFET gate periphery, each chip individually matched with its own input and output circuits. When the circuit was constructed in this way, the gain of the complete module was about the same as that which could be obtained from an individual chip, i.e., excellent size scaling was achieved.

The alternative procedure of matching a large gate periphery transistor with a single input and a single output circuit caused a considerable gain and power degradation over the former approach. In general we have found that multi-chip implementations have had clear performance advantages over large single-chip implementations.

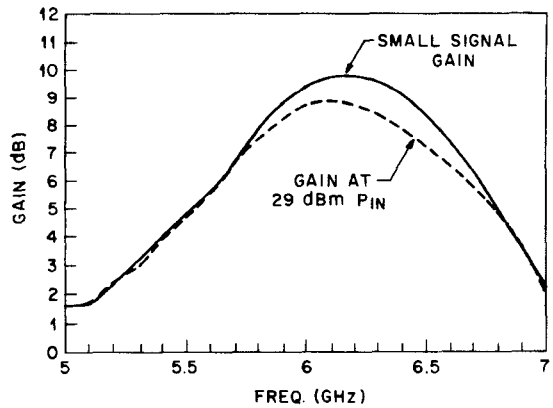


Fig. 4 6 GHz M-FET Performance

EXPERIMENTAL RESULTS

The 6 GHz M-FET contains two GaAsFET chips, each with a gate width of 6 mm and a gate length of 1.5 microns. The GaAsFETs, which are 38 microns thick, have a thermal impedance of 5 degrees C per watt. A number of M-FET modules have been assembled, adjusted, tested and found to perform well.

The yield of circuit chips in processing is better than 50 percent. That is, for every 100 possible circuit sites started on a wafer more than 50 of them produce DC-good circuit chips ready for use in M-FETs. An interesting component of the overall yield is the yield attributable to the capacitors. That yield is better than 90 percent.

A typical M-FET module (Fig. 4) with its drain biased at 13.5 volts and 1.3 amperes, operating at 1 dB gain compression, has 9 dB of gain at midband. This gain is achieved with an output power of 38 dBm or 6.3 watts. Bandwidth meets the design specification of 1 dB gain variation over 500 MHz and the compression characteristic is well behaved. At 1 dB compression the power gain of the M-FET is a few tenths of a dB better than that obtained from a single 6 mm device mounted in a standard package and measured using external coaxial tuners. Also, as noted above, excellent power scaling is observed in the 12 mm M-FET.

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